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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,386	10/30/2001	Mun-Mo Jeong	9898-188	5352

7590 02/13/2004

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/003,386	JEONG, MUN-MO	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-13,21,22,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 11-13, 21,22, 26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Sp cification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The amendment filed on 11/17/03 is objected to for including the limitation in claims 1 and 26 that the interconnection layer, the capping layer, and the etching stopper are formed by sequentially depositing material layers, and patterning the material layers by the same etching process. Nowhere in the specification applicant shows that the same etching process is used to etch the interconnection layer, the capping layer and the etching stopper layer There is

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4-9, 12-13, 21-22 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art in view of Urano JP patent No. 11077507.

Regarding claim 1, admitted prior art teaches (fig. 1) a method for manufacturing a semiconductor device comprising: forming plural interconnection layers (14) each including a capping layer (16) layer, the capping layer defining a contact resistance and on a semiconductor substrate (10); forming an interlayer insulating layer (18) overlying the interconnection layer (14); wherein the thickness of a portion of the interlayer

insulating layer on one of the capping layer is different from the thickness of a portion of the interlayer insulating layer on the others; etching the interlayer insulating layer (18) to form first contact holes therein.

Admitted prior art further teaches (fig. 1) the patterning of the ILD layer (12) the interconnection layer (14) and the capping layer (16) before forming the contact holes (20a), (20b) and (20c). Therefore admitted prior art inherently teaches the limitation of the interconnection layer, the capping layer, and the etching stopper are formed by sequentially depositing material layers, and patterning the material layers by the same etching process.

Admitted prior art does not teach the thickness of a portion of the interlayer insulating layer on one of the etching stoppers is different from the thickness of a portion of the interlayer insulating layer on the others; stopping etching when a top surface of each etching stopper is exposed; removing a portion of each etching stopper exposed by first contact holes, thereby forming second contact holes and leaving the capping layers of the plural interconnection layers at substantially the same thickness such that the contact resistance of the plural interconnection layers are substantially uniform; and forming a conductive layer within the second contact holes.

Urano teaches (figs. a-e) the use of TiN layer (capping layer 2) and an etch stop layer (8) to form contact holes through insulation layer with different thickness (see abstract) and forming a conductive layer (6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the etch stop layer taught by Urano in the process of

admitted prior art in order to form contact holes through insulation layer with different thickness.

The combined process of admitted prior art and Urano inherently forms second contact holes and leaves the capping layers of the plural interconnection layers at substantially the same thickness such that the contact resistance of the plural interconnection layers are substantially uniform.

Regarding claim 2, admitted prior art teaches (fig. 1) substantially the entire claimed process of claim 1 above including forming third contact holes (hole formed in layer 16) by slightly etching a portion of the capping layer (16) exposed by the second contact holes before forming the conductive layer, and wherein the conductive layer is formed within the second contact holes and the third contact holes.

The combined process of admitted prior art and Urano inherently forms third contact holes by slightly etching a portion of the capping layer exposed by the second contact holes before forming the conductive layer, and wherein the conductive layer is formed within the second contact holes and the third contact holes.

Regarding claim 4, admitted prior art teaches substantially the entire claimed method of claim 1 above including the conductive layer (6) is an upper interconnection layer filling the second and third contact holes and covering the top surface of the interlayer-insulating layer (fig. e, Urano).

Regarding claim 5, admitted prior art teaches substantially the entire claimed method of claim 1 above including the second and third contact holes are formed by

performing a dry etching method, using an etchant having a low etching selectivity between the etching stopper and the capping layer.

Since the combined process of admitted prior art and Urano is the same as the claimed process of the claimed invention and also since the layers of the combined structure of admitted prior art are the same as the claimed structure, the etchant would have a low etching selectivity between the etching stopper and the capping layer as claimed.

Regarding claim 6, admitted prior art teaches substantially the entire claimed method of claim 1 above including the etching stopper is formed of a nitride layer (8).

TiN nitride is a well-known anti-reflecting layer. Since Urano generally states that a nitride layer can be used as etching stopper layer, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use TiN as an etch stop layer.

Regarding claim 7, admitted prior art teaches substantially the entire claimed method of claim 1 above including the interconnection layer (6) is a metal layer containing aluminum (fig. e, Urano).

Regarding claim 8, admitted prior art teaches substantially the entire claimed method of claim 1 above including the capping layer (16) is formed of TiN (fig. 1, admitted prior art).

Regarding claim 9, admitted prior art teaches substantially the entire claimed method of claim 1 above including the interlayer-insulating layer is formed of silicon oxide layer (3) (col. 6, line 26).

Regarding claim 12, admitted prior art teaches substantially the entire claimed method of claim 1 above including the conductive layer is an upper interconnection layer filling the second contact hole and covering the top surface of the interlayer insulating layer (3) (fig. e, Urano).

Regarding claim 13, admitted prior art teaches substantially the entire claimed method of claim 1 above including the first contact hole is formed by using a dry etching method (col. 6, lines 33-34, Urano).

Regarding claim 21, admitted prior art teaches substantially the entire claimed method of claim 1 above including the capping layers are etched to form uniform thickness between the second contact holes.

Regarding claim 22, admitted prior art teaches substantially the entire claimed method of claim 1 above including the second contact holes expose a top surface of the capping layers.

Regarding claim 26, admitted prior art teaches (fig. 1) a method for manufacturing a semiconductor device comprising: forming plural interconnection layers (14) each including a capping layer (16) layer, the capping layer defining a contact resistance and on a semiconductor substrate (10); forming an interlayer insulating layer (18) overlying the interconnection layer (14); wherein the thickness of a portion of the interlayer insulating layer on one of the capping layer is different from the thickness of a portion of the interlayer insulating layer on the others; first etching the interlayer insulating layer (18) to form first contact holes therein.

Admitted prior art further teaches (fig. 1) the patterning of the ILD layer (12) the interconnection layer (14) and the capping layer (16) before forming the contact holes (20a), (20b) and (20c). Therefore admitted prior art inherently teaches the limitation of the interconnection layer, the capping layer, and the etching stopper are formed by sequentially depositing material layers, and patterning the material layers by the same etching process.

Admitted prior art does not teach the thickness of a portion of the interlayer insulating layer on one of the etching stoppers is different from the thickness of a portion of the interlayer insulating layer on the others; second etching a portion of each etching stopper exposed by the first contact holes, using a second etchant having a low etching selectivity between the etching stopper and the capping layer thereby forming second contact holes; and forming a conductive layer within the second contact holes.

Urano teaches (figs. a-e) the use of TiN layer (capping layer 2) and an etch stop layer (8) to form contact holes through insulation layer with different thickness (see abstract) and forming a conductive layer (6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the etch stop layer taught by Urano in the process of admitted prior art in order to form contact holes through insulation layer with different thickness.

Since the combined process of admitted prior art and Urano is the same as the claimed process and also since the layers of the combined structure of admitted prior art are the same as the claimed structure, the first etchant would have a high etching

selectivity between the etching stopper and the interlayer insulating film and the second etchant would have a low etching selectivity between the etching stopper and the capping layer as claimed.

Regarding claim 27, admitted prior art teaches substantially the entire claimed method of claim 26 above including stopping etching when a top surface of each etching stopper is exposed.

The claimed limitation above is an inherent property of an etch stop layer. Therefore admitted prior art inherently have the above claimed limitation.

4. Claims 3 and 11, are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted prior art and Urano in view of Bost et al. US patent No. 5,231,053.

Regarding claim 3, admitted prior art teaches substantially the entire claimed method of claim 1 above except explicitly stating that the conductive layer is formed only in the second and third contact holes.

Bost teaches (fig. 6 and 7) forming contact hole plug in contact hole (38), by etching back the blanket deposited plug material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of etching back the plug material taught by Bost in the process of admitted prior in order to ease subsequent metallization process.

Regarding claim 11, admitted prior art teaches substantially the entire claimed method of claim 1 above except explicitly stating that the conductive layer is formed only in the second contact hole.

Bost teaches (fig. 6 and 7) forming contact hole plug in contact hole (38), by etching back the blanket deposited plug material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of etching back the plug material in the process of admitted prior in order to ease subsequent metallization process.

Response to Arguments

5. Applicant's arguments with respect to claims 1-9, 11-13, 21-22 and 26-27 have been considered but they are not persuasive. Applicant argues that admitted prior art in view of Urano does not teach the limitation of the interconnection layer, the capping layer, and the etching stopper are formed by sequentially depositing material layers, and patterning the material layers by the same etching process. The above limitation is inherently taught by admitted prior art since forming contact holes inherently involves sequential patterning of interconnection layer, capping layer and etching stopper layer using the same etching process.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 305-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
February 8, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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